

**REMARKS**

The following remarks are submitted as a full and complete response to the outstanding Action. Currently, claims 4, 7 and 13-16 are pending in this application and submitted for reconsideration.

**Section 102 Rejection**

**Claims 4, 7 and 13-16 have been rejected under 35 U.S.C. §102(b) as being anticipated by Hazen et al. (U.S. Patent No. 5,280,447, hereinafter "*Hazen*").**

In the present application as set forth in claims 4, 7 and 13-16, the unit of erasure includes at least one but less than all of input/output terminals (i.e., the unit of erasure includes more than one but not all of the blocks, and the blocks respectively correspond to the input/output terminals).

The Examiner purports that the above claimed feature is shown in *Hazen*. Specifically, the Examiner states that one unit of erasure has 100a-100n sub-blocks, which is more than one block but not all blocks (100a-100n)-(115a-115n).

However, such assertion appears to be erroneous. *Hazen* teaches data bit groups (60a-60h) and (61a-61h), which correspond to respective data pins (i.e., respective I/O terminals) (see column 7, lines 16-25 of *Hazen*). Each of data bit sub-blocks in one data bit group belongs to one of the blocks. For example, a block BLOCK0 is formed by sub-blocks 100a, 101a through 115a in each of data bit groups (60a-60h) and (61a-61h) (see column 7, lines 26-39 of *Hazen*). During the block erasure operation, all the sub-blocks of a selected block are erased (see column 15, lines 5-16 of *Hazen*). That is, all the sub-blocks (e.g., 100a, 101a through 115a) of a selected block (BLOCK0),

which correspond to all the I/O terminals, are erased at once. In this manner, one unit of erasure is comprised of all the I/O terminals. This is also the case even when the configuration information is provided (see column 15, lines 17-32 of **Hazen**).

Accordingly, it is respectfully submitted that **Hazen** does not teach or suggest the unit of erasure that includes more than one but not all of input/output terminals as presently set forth in claims 4, 7 and 13-16.

#### Section 103 Rejections

**Claims 13 and 15 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hazen in view of Honda et al. (U.S. Patent No. 6,377,502, hereinafter "Honda").**

**Honda** does not supplement for the above-discussed deficiency in **Hazen** with respect to the unit of erasure that includes more than one but not all of input/output terminals as presently set forth in claims 4 and 7 from which claims 13 and 15 respectively depend.

**Claims 14 and 16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hazen in view of Liu (U.S. Patent No. 6,549,474).**

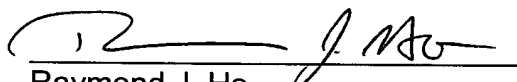
**Liu** does not supplement for the above-discussed deficiency in **Hazen** with respect to the unit of erasure that includes more than one but not all of input/output terminals as presently set forth in claims 4 and 7 from which claims 14 and 16 indirectly depend.

In view of the above remarks, the Applicants respectfully submit that each of claims 4, 7 and 13-16 recites subject matter which is neither disclosed nor suggested in the cited prior art. Applicants therefore request that each of claims 4, 7 and 13-16 be found allowable, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,

  
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